AQ – 2796

Second Semester M. E. Full Time (Digital Electronics) CGS Examination

PARALLEL COMPUTING

2 UMEE 3

P. Pages : 3

Time : Three Hours] [Max. Marks : 80

Note : (1) Due credit will be given to neatness and adequate dimensions.
(2) Assume suitable data wherever necessary.
(3) Diagrams and Chemical equations should be given wherever necessary.
(4) Illustrate your answer wherever necessary with the help of neat sketches.
(5) Use pen of Blue/Black ink/refill only for writing the answer book.

1. (a) Explain the Flynn's classification of computers architecture with the help of neat diagrams. 7

(b) Use Bernstein's conditions to determine the parallelism in following instructions

$I_1 : x = (a + b) / (a * b)$

$I_2 : y = (b + c) * d$

$I_3 : z = x^2 + (a * e)$ 6

OR

2. (a) Differentiate between UMA , NUMA and COMA. 7

(b) Explain the following in brief :—

(i) Clock rate and CPI (ii) MIPs rate (iii) Throughput rate. 6

3. (a) Explain various grain sizes with respect to program partitioning for scheduling. 7

(b) Explain the following static connection networks :—

(i) Linear Array (ii) Binary Fat tree (iii) Hypercube. 6

OR

4. (a) Explain in brief demand driven mechanism. 7

(b) Explain the following with respect to dynamic connection network

(i) Digital buses (ii) Multistage network (iii) Baseline network. 6

5. (a) Discuss in brief the asynchronous and synchronous pipeline mode. Also explain clock skewing. 6

(b) Consider the following pipeline reservation table.

	1	2	3	4
S1	X			X
S2		X		
S3			X	

(i) What are the forbidden latencies.

(ii) List all simple and greedy cycles.

(iii) Determine the optimal constant latency cycle and the minimal average latency.

(iv) Let the pipeline clock period be τ = 20 ns. Determine the throughput of the pipeline. 8

OR

6. (a) Explain the difference between superscalor and superpipeline design with the help of suitable diagram. 8

(b) Consider the execution of a program of 15000 instruction by linear pipeline processor. The clockrate of a pipeline is 25 MHz. Pipeline has five stages and one instruction is to be issued per clock cycle. Neglect penalties due to branch instruction and out of sequence execution

(i) Calcualte the speedup program execution by pipeline as compared with that by non pipeline processor.

(ii) What are the efficiency and throughput of the pipeline processor. 6

7. (a) Explain the interconnection structure in a generalized multiprocessor system with local memory, private caches, shared memory and shared pipeline. 8

(b) Explain in brief a cross point switch design in a crossbar network. Enlist the advantages of cross bar network. 6

OR

8. (a) Explain in brief the following directory based protocols.

(i) Full map directories (ii) Limited directories. 8

(b) Explain in brief message format in message routing schemes. Also explain store and Forward routing and Wormhole routing. 6

9. (a) Discuss in brief a realable coherent cache multiprocessor with distributed stored memory. 7

(b) Discuss in brief the message driven processor architecture. 6

OR

10. (a) Discuss the effect of using a relaxed consistancy memory model in a scalable multiprocessor with multi threading. 7

(b) What do you mean by efficiency of a processor. Discuss in brief the processor efficiency in

(i) Saturation region (ii) Linear region. 6

11. (a) Explain the following as applied to parallel programming environment

(i) Visuallization support (ii) Performance tunning. 7

(b) Differentiate between message passing programming model and shared memory programming model. 6

OR

12. (a) Discuss synchronization mechanism for interprocess communication with the help of basic operation. 7

(b) Discuss in brief :—

(i) Multitasking (ii) Autotasking.

as applied to multi processing environment. 6