AQ–2800

Faculty of Engineering & Technology

M.E. (Digital Electronics) (Part Time/Full Time) Semester-II (C.G.S.-New) Examination

Elective-II

HIGH SPEED DIGITAL SYSTEM DESIGN

Paper—2 UMEF 5

Sections—A & B

Time—Three Hours] [Maximum Marks—80

INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.

(2) Answer **THREE** questions from Section A and **THREE** questions from Section B.

(3) Due credit will be given to neatness and adequate dimensions.

(4) Assume suitable data wherever necessary.

(5) Illustrate your answers wherever necessary with the help of neat sketches.

(6) Use pen of Blue/Black ink/refill only for writing the answer book.

SECTION—A

1. (a) Describe the near-end and far-end cross talk. How is the cross talk affect the system level timing and the integrity of the signal ? 7

   (b) Explain different termination schemes to eliminate reflections in transmission lines. 7

2. (a) Explain odd and even mode propagation in case of transmission line pair. Determine the equivalent inductance and equivalent capacitance equations. 7

   (b) Calculate multiple reflections for an underdriven open transmission line using lattice diagram, if γ_s = 0—2 V, z_o = 50 ohms, Time Delay = 250 ps. Assume z_s = 75 ohms. Plot response from lattice diagram. 7

3. (a) Explain frequency dependent losses in microstrips and strip lines. 6

(b) Explain the common types of packages with respect to the following points :

(i) Attachment of the die to the package

(ii) On-package connections and

(iii) Attachment of the package to the PCB. 7

4. (a) Explain non-ideal current return paths for the :

(i) Signals transversing a ground gap

(ii) Signals changing reference planes

(iii) Signal referenced to power or ground plane. 7

(b) Explain effects of inductively coupled connector pin fields. 6

SECTION—B

5. (a) Draw and explain the block diagram of common clock timing technique. Derive the timing equations from timing diagram of common clock bus. 7

(b) Explain the operation of the CMOS output buffer when input voltage is :

(i) high and

(ii) low. 6

6. (a) Explain the flow chart of efficient bus design methodology for high speed digital system design. 7

(b) Explain the concept of Flight Time. Explain the process of flight skew calculation between data and strobe. 7

7. (a) Explain the following parameters related with the digital oscilloscopes :

(i) Bandwidth

(ii) Sampling. 6

(b) Explain the different decoupling and chocking methods in a high speed digital circuits. 7

8. (a) Explain the VNA calibration procedure with VNA sources of errors using VNA one port error model. 7

(b) Explain Time Domain Reflectometry (TDR) measurement factors that affect TDR resolution. 7