**AQ–2874**

**Faculty of Engineering & Technology**

**M.E. Electrical & Elect. Semester-II (New-CGS) Examination**

**EMBEDDED SYSTEMS DESIGN**

**Paper—2 EEEME 2**

**Sections—A & B**

Time—Three Hours] [Maximum Marks—80

**INSTRUCTIONS TO CANDIDATES**

(1) All questions carry marks as indicated.

(2) Answer **THREE** questions from Section A and **THREE** questions from Section B.

(3) Assume suitable data wherever necessary.

(4) Illustrate your answers wherever necessary with the help of neat sketches.

(5) Use pen of Blue/Black ink/refill only for writing the answer book.

**SECTION—A**

1. (a) Compare the annual rate growth of :

   (a) IC capacity

   (b) Designer productivity. 6

   (b) Explain port pin circuits of Port 0, Port 1 and Port 3. 8

**OR**

2. (a) If Moore's law continues to hold, predict the approximate number of transistor per leading edge IC in the year :

   (i) 2030

   (ii) 2050. 7

   (b) Differentiate general purpose processor, single purpose processor and ASIC with respect to design matrix, with suitable example. 7

(Contd.)

3. (a) Build a 2-input :
   (i) AND Gate
   (ii) OR Gate using minimum no. of transistors. 6

   (b) Describe different RT level combinational and sequential components used to design single function processor. 7

**OR**

4. (a) Four lights are connected to decoder built a circuit that will blink light in following order : 0, 2, 1, 3, 0, 2 ...... starts from state diagram, state table, minimize the logic and draw the final circuit. 7

   (b) Design a 3 bit counter that counts following sequence : 1, 2, 4, 5, 7, 1, 2, .....
   The counter has an output "EVEN" whose value is one when the current count value is EVEN. Use the sequential design technique. 6

5. (a) Explain data transfer mechanism in $I^2C$ protocol. Compare it with CAN and USB protocols based on the bit rate and area of application. 7

   (b) Compare 1K × 8 ROMS into an 8K × 8 ROM. 6

**OR**

6. (a) Draw and explain cache mapping techniques. 7

   (b) Explain daisy chain arbitration. 6

## SECTION—B

7. (a) What is data flow model ? Give suitable example. 6

   (b) Explain finite state machine and concurrent process with suitable example. 7

**OR**

8. (a) Explain :
   (i) Logic synthesis
   (ii) RT synthesis
   (iii) Behavioural synthesis. 8

   (b) Explain different models that are used to describe embedded systems. 5



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9. (a) Explain the role of schedular in RTOS. Compare preemptive and non-preemptive scheduling techniques. 7
   (b) Explain interrupt routines in RTOS environment. 6

**OR**

10. (a) Explain Rate Monotonic Analysis (RMA), in scheduling. 7
    (b) How mailbox message is different from qucue message ? 6

11. (a) List and explain various functions supported by Linux/RT Linux. 9
    (b) Explain Host/target linked setup. 5

**OR**

12. In relation to Embedded Linux, how TCPIP networking is done ? Explain network configuration. 14