

AQ-2790

Faculty of Engineering & Technology  
M.E. Semester—I [Full Time] (Digital Electronics) (C.B.S.) Examination  
RF SYSTEM DESIGN

Elective—I

Paper—I UMEF 3

Sections—A & B

Time : Three Hours]

[Maximum Marks : 80

INSTRUCTIONS TO CANDIDATES

- (1) All questions carry marks as indicated.
- (2) Answer **THREE** questions from Section A and **THREE** questions from Section B.
- (3) Due credit will be given to neatness and adequate dimensions.
- (4) Assume suitable data wherever necessary.
- (5) Illustrate your answers wherever necessary with the help of neat sketches.
- (6) Use pen of Blue/Black ink/refill only for writing the answer book.

SECTION—A

1. (a) Explain the frequency response of RF field effect transistors. 7  
(b) Explain the small signal BJT model. 7
2. (a) Explain the construction and functionality of High Electron Mobility Transistors. 7  
(b) For a particular Si pn-junction the doping concentrations are given to be  $N_A = 10^{18} \text{ cm}^{-3}$  and  $N_D = 5 \times 10^{15} \text{ cm}^{-3}$  with an intrinsic concentration of  $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$ . Find the barrier voltages for  $T = 300^\circ\text{K}$ . 6
3. (a) Discuss a method used to convert lumped elements to transmission line sections. 7  
(b) Explain the design of class A power amplifier. 6

4. (a) Explain Bandwidth enhancement in high frequency amplifier design. 7  
 (b) Explain the following related to filter implementation :  
 (i) Unit elements 6  
 (ii) Huroda's Identities.

### SECTION—B

5. (a) Explain in brief single-ended LNA and differential LNA design. 6  
 (b) Explain the following characteristics of a mixer :  
 (i) Conversion gain 8  
 (ii) Noise figure 7  
 (iii) Linearity and isolation 6  
 (iv) Spurs. 7
6. (a) Explain linearity and large-signal performance in LNA. 6  
 (b) Explain dielectric resonator oscillator design. 7
7. (a) Explain noise properties of PLLs. 6  
 (b) Explain second-order PLL model. 7
8. (a) What are sequential phase detectors ? Hence, explain SR flip-flop as a phase detector. 7  
 (b) Explain the following related to PLL design :  
 (i) Loop filters 6  
 (ii) Charge pumps.