AQ – 2871

First Semester M. E. (Electrical and Elect.) Examination

VLSI DESIGN

1 EEEME 4

P. Pages : 3

Time : Three Hours] [Max. Marks : 80

Note : (1) Separate answer book must be used for each section in the subject Geology, Engineering material of civil branch and Separate answer-book must be used for Section A and B in Pharmacy and Cosmetic Tech.
(2) Answer **Three** questions from Section A and **Three** questions from Section B.
(3) Due credit will be given to neatness and adequate dimensions.
(4) Assume suitable data wherever necessary.
(5) Illustrate your answer wherever necessary with the help of neat sketches.
(6) Use pen of Blue/Black ink/refill only for writing the answer book.

SECTION A

1. (a) Explain the skin effect in copper interconnects. What are the various ways of reducing this effect ? 7

(b) Draw and explain a typical design abstraction ladder for digital systems. 7

OR

2. (a) Discuss the design-and-conquer approach of chip design using suitable example. 7

(b) Discuss the various CMOS layout design and analysis tools. 7

3. (a) Draw and explain the τ model of estimating the transition time. If values of R_n and C_L are 6.47 kΩ and 1.78 fF, what would be the fall time ? 8

(b) Describe the various sources of power dissipation in CMOS circuits and enlist ways of power economy. 5

OR

4. (a) Calculate the no. of buffers required when a minimum size inverter drives a metal 1 wire that is 20,000λ x 3λ. The RC values are R_0 = 6.47 KΩ. Co = 1.78 fF, Rint = 533 Ω, Cint = 212 fF. Also compute the 50% delay. 8

(b) What is 'Design for yield' ? Explain the various techniques of design for yield. 5

5. (a) Explain the different techniques of cross talk minimization. 7

(b) How would you factorize a function $f = ab + bc + cd$ so as to get minimum glitches in the output ? Explain. 6

OR

6. (a) Explain gate testing with respect to

(i) Fault models

(ii) Stuck-at-0/1 fault

(iii) Testing difficulty

(iv) Limitations of fault model.

(v) Stuck-open model and

(vi) Delay fault model. 13

SECTION B

7. (a) Draw the block diagram for a four-bit counter with LSSD scan chain. 7

(b) Discuss the one-phase and two-phase systems for latches and highlight the adavnatges and disadvantages of each. 7

OR

8. (a) What is 'clock skew' ? What are the various ways of minimizing the clock skew ? 7

(b) Draw the block diagram and explain the use of PLL in clock generation. 7

9. (a) What are 'active pixel sensors' ? Explain the working with neat diagram. 6

(b) Explain booth encoding to speed up multiplication. Draw the structure. 7

OR

10. (a) Explain the Wallace tree structure. How is multiplication speeded up in wallace tree ? 7

(b) What is FPGA ? Explain the structure of a typical FPGA and highlight the applications of FPGA. 6

11. (a) What are the challenges in clock distribution across the chip ? Explain the H tree and enlist its advantages. 7

(b) What is the need of validation during chip assembly ? Explain. 6

OR

12. (a) What is 'Global Routing' ? Why is it necessary to go through the placement-global routing cycle several times ? 7

(b) State the properties of a desired I/O subsystem and Explain the power supply, Input/output bidirectional and analog pads. 6