M.E. Second Semester (Digital Electronics) (Part Time / Full Time) (C.G.S.- New)

13231 : CMOS VLSI Design : 2 UMEF 2

P. Pages : 2 | AU - 3323

Time : Three Hours | Max. Marks : 80

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Notes : 1. Answer **three** question from Section A and **three** question from Section B.
2. Due credit will be given to neatness and adequate dimensions.
3. Assume suitable data wherever necessary.
4. Diagrams and design equations should be given wherever necessary.
5. Illustrate your answer necessary with the help of neat sketches.
6. Use of pen Blue/Black ink/refill only for writing the answer book.

SECTION - A

1. Discuss with suitable examples the following CMOS testing methods : **14**

i) Observability & controllability

ii) Functionality & Manufacturing test

OR

2) Explain the scan - design strategy for testing. Also discuss the following scan - based testing methods : **14**

i) Parallel - scan.

ii) Scanable - Register Design

3. With the help of neat diagrams, explain how barrel - shifter performs rotate - right, rotate - left & shift operations. Also develop the design of 32 - bit logarithmic barrel - shifter. **13**

OR

4. a) Explain the trade - offs between open, closed & twisted bit lines in a dynamic RAM array. **7**

b) Design a Gray - coded counter in which only one - bit changes on each - cycle. **6**

5. Briefly discuss the speed limitations of comparator circuit. Discuss the design of high - speed comparator using a combination of preamplifier followed by a latch. The preamplifier uses bandwidth to quickly build up the input. The latch uses positive feedback to take the signal to its final. **13**

OR

6. With the help of neat circuit diagram & associated design equations, explain the behaviour of switch capacitor filters. **13**

SECTION - B

7. With reference to CMOS PLL, explain the following blocks with their design equations : **13**

   i) Phase - Frequency detector.

   ii) Charge - pump & loop fibre.

   iii) VCO

   iv) Compare the performance parameters of current starved & LC oscillator based VCO.

OR

8. Design class - E RF power - amplifier for following specifications : **13**

   i) Load 1 W, 50 ohm

   ii) DC supply = 3.3 V.

   iii) Q = 10

   Briefly, describe the circuit behaviour along with the design equations used.

9. Explain in detail the I/O planning, power planning & clock planning after floorplanning in ASICS. **13**

OR

10. a) Explain the look - ahead partitioning algorithm & enlist the merits over K - L algorithm. **7**

    b) Explain briefly the various sources of power - dissipation in CMOS ASIC design. **6**

11. Briefly explain the goals & objectives of placement process in ASIC design. Also, explain in detail the zero - stack algorithm. **14**

OR

12. a) Describe SDF, PDEF, LEF & DEF formats for floorplanning & placements. **7**

    b) Briefly discuss to physical design flow related to floorplanning and placement in ASIC design. **7**

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