M.E. First Semester (Digital Electronics) (Part Time / Full Time) (C.G.S.- New)

13204 : Elective - I : RF System Design : 1 UMEF 3

P. Pages : 1 **AU - 3318**

Time : Three Hours * 0 8 1 4 * Max. Marks : 80

Notes : 1. Answer **three** question from Section A and **three** question from Section B.
2. Due credit will be given to neatness and adequate dimensions.
3. Diagrams and Chemicals equations should be given wherever necessary.
4. Illustrate your answer necessary with the help of neat sketches.

SECTION - A

1. a) Explain the construction and functionality of Modulation Doped FET. **7**

b) A GaAs MOSFET has following parameter. **6**

$N_D = 10^{16} cm^{-3}$, $d = 0.75\ \mu m$, $w = 10\ \mu m$, $L = 2\mu m$, $Er = 12.0$, $V_d = 0.8V$

and $\mu_n = 8500\ cm^2 / Vs$

Determine:

i) Pinch-off voltage ii) Threshold voltage

iii) Maximum Saturation current.

2. a) Explain large signal BJT model. **7**

b) Discuss the limiting values of BJT and MOSFET in details. **7**

3. a) Discuss the insertion loss method of RF filter design. **7**

b) Compare Butterworth and Chebyshev filter. **6**

4. a) Explain the concept of HF cascade amplifier design. **6**

b) What are the switched mode power amplifiers ? Hence explain the operation of 'Class F' RF power amplifier. **7**

SECTION - B

5. a) Explain the design of dielectric resonator oscillator. **6**

b) Explain the LNA topologies and design in detail. **8**

6. a) Explain the concept of subsampling mixer along the diagram. **6**

b) Explain the circuit of varactor diode oscillator with Pi-type feedback loop. **7**

7. a) Explain second order PLL model. **6**

b) Explain the communicating multiplier as a phase detector. **7**

8. a) Along with the circuit diagram explain the concept of S-R Flip-Flop as a sequential phase detector. **7**

b) Explain PLL charge pump. **6**

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