M.E. First Semester (Electrical & Elect.Engg.) (New-CGS)

13284 : VLSI Design : 1 EEEME 4

P. Pages : 2 | AW - 3568

Time : Three Hours | Max. Marks : 80

Notes :
1. Due credit will be given to neatness and adequate dimensions.
2. Assume suitable data wherever necessary.
3. Diagrams and equations should be given wherever necessary.
4. Illustrate your answer necessary with the help of neat sketches.
5. Use of pen Blue/Black ink/refill only for writing the answer book.

SECTION – A

1. a) For the following design rules give the reasoning. **8**
- i) Overhang of poly at transistor gate.
- ii) Metal 1 surround of via cut
- iii) Tub overhang
- iv) Poly diffusion spacing.
- v) Via-cut-via cut spacing.

b) Explain CMOS technology and highlight its features over other technologies. **6**

OR

2. a) What is the need of IP based design? What are types of IP? Discuss IP life cycle in detail. **8**

b) Why metal-metal spacing is larger than poly-poly spacing? Explain. **6**

3. a) Explain general principle of CMOS implementation of a multiplier. **7**

b) A 3 – input majority gate returns a true output if at least two of the inputs are true. A minority gate is its complement. Design a 3-input CMOS minority gate using a single state of logic. Sketch a transistor level schematic and its stick diagram. **6**

OR

4. a) Draw and explain the τ model of estimating the transition time. If values of R_n and C_L are 6.47kΩ and 1.78 f F, what would be the fall time? **8**

b) Describe the various sources of power dissipation in CMOS circuits and enlist ways of power economy. **5**

5. a) Explain the different techniques of cross talk minimization. **7**

b) Explain combinational network testing. **6**

OR

6. Explain gate testing with respect to : **13**
- i) Fault models
- ii) Stuck-at- 0/1 fault
- iii) Testing difficulty
- iv) Limitations of fault model
- v) Stuck – open model and
- vi) Delay fault model.

SECTION – B

7.	a)	Explain with example state assignment.	7
	b)	What is clock skew? Is a single phase or two phase system more sensitive to clock skew; justify your answer.	7

OR

8.	a)	Explain and compare the following methods of sequencing blocks of combinational logic. i) Flip flop based system. ii) 2 – phase system iii) Pulsed system.	8
	b)	What is scan design? Explain.	6
9.	a)	Explain how 3T DRAM is different from 1T DRAM with relevant figures.	7
	b)	Discuss in detail the image sensor architectures.	6

OR

10.	a)	Explain implementation of MUX based ALU.	7
	b)	Draw and explain the operation of barrel shifter.	6
11.	a)	Explain with example the issues related with: i) I/O planning. ii) Power planning. iii) Clock planning	7
	b)	What is the need of validation during chip assembly? Explain.	6

OR

12.	a)	Discuss various techniques that can be used to reduce and manage power consumption.	7
	b)	Discuss clock generation and clock distribution with respect to floor planning.	6

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