M.E. Second Semester (Digital Electronics) (Part Time / Full Time) (C.G.S.- New)

13232 : Parallel Computing : 2 UMEF 3 / 4 UMEP 1

P. Pages : 2 **AW - 3764**

Time : Three Hours * 1 0 6 2 * Max. Marks : 80

Notes : 1. Due credit will be given to neatness and adequate dimensions.
2. Assume suitable data wherever necessary.
3. Illustrate your answer necessary with the help of neat sketches.
4. Use of pen Blue/Black ink/refill only for writing the answer book.

1. a) Give Flynn's classification of various computer architectures. Clearly explain the features of each with conceptual diagrams. **7**

b) A 40 MHz processor was supposed to execute 200000 instructions with following instruction mix and CPI needed for each instruction. Determine the effective CPI, MIPS rate and execution time. **7**

Instruction type	CPI	Instruction count
Integer arithmetic	2	60%
Data transfer	4	18%
Floating point	6	12%
Control transfer	5	10%

OR

2. a) Differentiate between implicit and explicit parallelism with a neat sketch. **7**

b) Explain different types of data dependency with an example. Draw the data dependency graph for the following. **7**
S1: Load R1, M(200)
S2: Move R2, R1
S3: Inc R1
S4: Add R2, R1
S5: Store M(200), R1

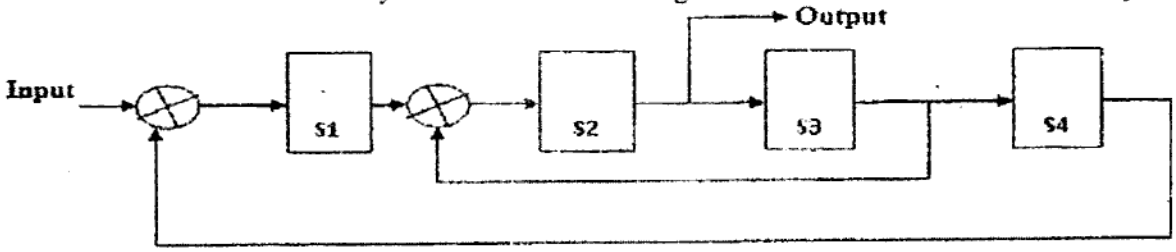
3. Explain how grain packing can be done to compute the sum of the 4 elements in the resulting product matrix $C = A \times B$. Where A and B are 2×2 matrices. Assume grain size for multiplication is 101 and the grain size for addition is 8. **13**

OR

4. a) Compare control flow verses dataflow mechanism with necessary diagram. **7**

b) Explain the following static connection networks. **6**
i) Linear Array ii) Binary flat tree and iii) Hyper cube

5. Consider the following pipelined processor with four stages. This pipeline has a total evaluation time of six clock cycles. All successor stages must be used after each clock cycle. **13**



i) Specify the reservation table for this pipeline with six columns and four rows.
ii) List the set of forbidden latencies between task initiations.

iii) Draw the state diagram which shows all possible latency cycles.
iv) List all greedy cycles from the state diagram.
v) What is the value of minimal average latency (MAL)?

OR

6. Differentiate between: **13**
i) Super scalar processors and VLIW processors.
ii) Trace scheduling and dynamic scheduling.
iii) Software pipelining and hardware pipelining.

7. a) What is the cache coherence and why is it important in shared memory multiprocessor system? How can the problem be solved with snoopy cache controller? **7**

b) What do you mean by virtual channels? Explain in brief the deadlock avoidance techniques. **7**

OR

8. a) Explain in brief the following directory based protocols. **7**
i) Full map directories. ii) Limited directories.

b) Explain in brief the Goodman's write once cache coherence protocol. **7**

9. a) Distinguish between. **8**
i) Multiprocessor and Hyperthreading technology.
ii) Hardware based and software based multithreading.

b) Discuss the features of message driven processor, making it suitable for building fine grains multicomputer. **5**

OR

10. a) Discuss the effect of using a relaxed consistency memory model in a scalable multiprocessor with multi threading. **7**

b) What do you mean by efficiency of a processor. Discuss in brief the processor efficiency in **6**
i) Saturation region. ii) Linear region.

11. a) Explain the following as applied to parallel programming environment. **7**
i) Visualization support. ii) Performance tuning.

b) Differentiate between passing programming model and shared memory programming model. **6**

OR

12. a) Discuss synchronization mechanism for inter-process communication with the help of basic operation. **7**

b) Discuss in brief as applied to multi-processing environment. **6**
i) Multitasking ii) Auto - tasking.

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