M.E. Second Semester (Digital Electronics) (Part Time / Full Time) (C.G.S.- New)

13231 : CMOS VLSI Design : 2 UMEF 2

P. Pages : 2

Time : Three Hours

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AW - 3763

Max. Marks : 80

Notes : 1. Due credit will be given to neatness and adequate dimensions.
2. Assume suitable data wherever necessary.
3. Illustrate your answer necessary with the help of neat sketches.
4. Use of pen Blue/Black ink/refill only for writing the answer book.

1. a) Draw and explain the basic CMOS layout of a NOR gate. **7**

b) What is Automatic-Test-Pattern-Generation (ATPG)? Explain with suitable example. **7**

OR

2. a) How is Serial-Scan testing implemented? Explain. **7**

b) What is meant by Stuck-At-1 fault & Stuck-At-0 fault? Explain with suitable example. **7**

3. a) Explain the working of carry-look ahead adder. Also give its advantages over ripple carry adders. **5**

b) Implement the function $P = A \oplus B \oplus C \oplus D$ using static 4-input XOR gate and explain in brief. **8**

OR

4. a) Draw & briefly explain the structure of a 4×4 array multiplier. **8**

b) What is Content-Addressable Memory (CAM)? Draw & explain the typical CAM cell. **5**

5. a) Draw the schematic of a switched capacitor comparator & list the advantages & disadvantages over an open-loop comparator having the same gain and frequency response. **6**

b) Explain how the shape of the input waveform to a CMOS logic alters the delay through the gate. **7**

OR

6. a) How is capacitance estimated in CMOS device? Explain. **6**

b) Give the specifications of a typical high speed comparator & list the applications. **7**

7. a) With reference to the simplified model of Colpitts oscillator [Fig 7 (a)] show that the amplitude of the tank voltage, $V_{tank} = 2I_{BIAS} \cdot R \cdot (1-n)$ where n is the capacitive voltage divider factor. 7

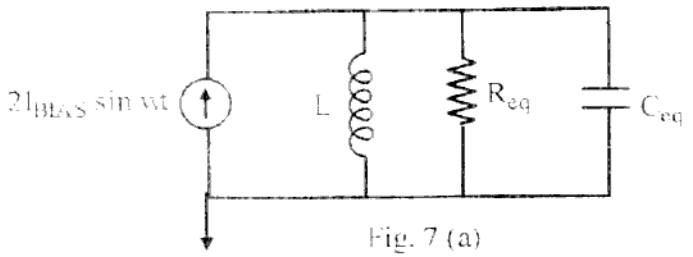

Fig. 7 (a)

b) 'In PLL, an analog multiplier can be used as a phase detector', Justify with necessary proof & equations. 7

OR

8. a) A linear amplifier used in a 1 GHz communication system need to supply 1 watt into 50Ω load resistor. With necessary load impedance transformation, compute the drain efficiency of the amplifier. Assume that a 3.3V dc supply is available. 10

b) What is thermal runaway? Explain. 4

9. a) Draw the block diagram and explain the typical ASIC design flow. 5

b) Explain the Kernighan-Lin FPGA partitioning algorithm. 8

OR

10. a) Explain the various sources of power dissipation in CMOS logic. 6

b) What is FPGA partitioning? Explain any one method of partitioning. 7

11. a) What is 'Nanoscale technology'? Explain in brief. 6

b) What is design rule check (DRC)? Explain 'Phantom level DRC' and 'Layout Versus Schematic (LVS) check in brief. 7

OR

12. a) List the various global routing methods & explain in brief. 6

b) Draw the schematic & explain timing-driven floorplanning & placement design flow. 7

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