M.E. Second Semester (Digital Electronics) (Part Time / Full Time) (C.G.S.- New)

13232 : Parallel Computing : 2 UMEF 3 / 4 UMEP 1

P. Pages : 2 | **AU - 3324**

Time : Three Hours | Max. Marks : 80

* 0 9 4 6 *

Notes : 1. Due credit will be given to neatness and adequate dimensions.
2. Assume suitable data wherever necessary.
3. Illustrate your answer necessary with the help of neat sketches.
4. Use of pen Black ink/refill only for writing the answer book.

1. a) Explain various speedup performance laws with their basis of application. **7**

b) A non - pipelined processor X has a clock rate of 25 MHz and an average CPI of 4. Processor Y, an improved successor of X, is designed with a five stage linear instruction pipeline. However, due to the latch delay and clock skew effects the clock rate of Y is only 20 MHz. **7**
i) If a program containing 100 instructions is executed on both processors. What is the speedup of processor Y compared with that of processor X ?
ii) Calculate the MIPS rate of each processor during the execution of this particular program.

OR

2. a) Differentiate between implicit and explicit parallelism with a neat sketch. **7**

b) Explain different types of data dependency with an example. Draw the data dependency graph for the following : **7**
S1 : Load R1, M(1000)
S2 : Move R2, R1
S3 : Inc R1
S4 : Add R2, R1
S5 : Store M(1000), R1

3. Explain how grain packing can be done to compute the sum of the 4 elements in the resulting product matrix C = A x B. Where A and B are 2 x 2 matrices. Assume grain size for multiplication is 101 and the grain size for addition is 8. **13**

OR

4. a) Explain the various grain sizes with respect to program partitioning for scheduling. **7**

b) Explain the following static connection networks. **6**
i) Linear array,
ii) Binary Flat tree and
iii) Hyper cube

5. a) Consider the execution of a program of 15,000 instructions by a linear pipeline processor with a clock of 25 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and cut-of-sequence executions are ignored. **7**

i) Calculate the speedup factor using the pipeline to execute the program as compared with the use of equivalent non-pipelined processor with an equal amount of flow-through delay.
ii) What are the efficiency and throughput of this pipelined processor ?

b) Explain speedup, efficiency and throughput for a pipeline processor. 6

OR

6. Differentiate between : 13
i) Super scalar processors and VLIW processors.
ii) Trace scheduling and dynamic scheduling.
iii) Software pipelining and hardware pipelining.

7. a) What is the cache coherence and why is it important in shared memory multiprocessor system ? How can the problem be solved with snoopy cache controller ? 7

b) What do you mean by virtual channels ? Explain in brief the deadlock avoidance techniques. 7

OR

8. a) Explain in brief the following directory based protocols. 7
i) Full map directories ii) Limited directories

b) Explain the following terms as applied to communication patterns in a message passing network : 7
i) Unicast versus multicast
ii) Broadcast versus conference

9. a) Distinguish between : 8
i) Multiprocessor and Hyper threading technology.
ii) Hardware based and software based multithreading.

b) Explain the context switching policies in multithreaded architecture. 5

OR

10. a) Differentiate between static dataflow computer and dynamic dataflow computer. 7

b) Explain the principle of multithreading. 6

11. a) Explain the following as applied to parallel programming environment. 7
i) Visualization support
ii) Performance tuning

b) Differentiate between passing programming model and shared memory programming model. 6

OR

12. a) Explain in detail as applied to the multiprocessing environment. 7
i) Multitasking
ii) Autotasking
iii) Microtasking

b) Explain the term heterogeneous processing. 6

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